IN THE CLAIMS

1. (Currently Amended) A memory device comprising:

an input node for receiving an external signal;

a memory array having row and column of memory cells;

a row decoder connected to the memory device;

a column decoder connected to the memory device;

a plurality of measuring delay elements connected to the input node for delaying the external signal during a measurement to produce a measured delay, wherein the measurement is set to last for at least one cycle time of the external signal;

an interval controller connected between the input nodes and the measuring delay elements for controlling the frequency of the measurement;

a plurality of correction delay elements connected to the input node for delaying the external signal based on the measured delay to generate an internal signal; and

an output data path circuit connected to the memory array and the plurality of the correction delay elements for receiving the internal signal to control data transfer from the memory array.

2. (Currently Amended) A memory device comprising:

an input node for receiving an external signal;

a memory array having row and column of memory cells;

a row decoder connected to the memory device;

a column decoder connected to the memory device;

a plurality of measuring delay elements connected to the input node for delaying the external signal during a measurement to produce a measured delay;

an interval controller connected between the input nodes and the measuring delay elements for controlling the frequency of the measurement;

a plurality of correction delay elements connected to the input node for delaying the external signal based on the measured delay to generate an internal signal; and

an output data path circuit connected to the memory array and the plurality of the correction delay elements for receiving the internal signal to control data transfer from the memory array ~~The memory device of claim 1~~, wherein the interval controller includes a frequency modifier for setting a time interval between one measurement and the next measurement to be unequal to a cycle time of the external signal.

3. (Currently Amended) The memory device of claim [[1]] 2, wherein the frequency modifier includes a frequency divider to divide the frequency of the external signal.

4. (Original) The memory device of claim 3, wherein interval controller further includes a frequency shifter for shifting signals produced by the frequency divider.

5. (Currently Amended) A memory device comprising:

input nodes for receiving input signals and an external signal;

a memory array for storing data;

a decoding circuit for decoding the input signals to access the data;

an output data path circuit connected to the memory array for transferring the data; and

a delay locked circuit connected to the input nodes and the data output path the delay [[lock]] locked circuit including:

a measuring unit located on a first path for generating a measured delay based on at least one measurement on timing of the external signal on the first path, wherein the measurement is set to last for at least one cycle time of the external signal;

an interval controller located on the first path, the interval controller is configured to control a frequency of the measurement to be unequal to a frequency of the external signal; and

an adjusting unit located on a second path for delaying the external signal to generate and internal signal based on the measured delay, the adjusting unit including an output node connected to the output data path for providing the internal signal to the output data path circuit to control a transfer of the data between the memory array and the output data path circuit.

6. (Original) The memory device of claim 5, wherein the measuring unit includes a delay model connected to an output node of the interval controller for delaying a signal outputted at the output node of the interval controller.

7. (Original) The memory device of claim 6, wherein the measuring unit includes a converter connected between the output node of the delay model and the adjusting unit for converting a reference time into the measured delay.

8. (Currently Amended) A memory device comprising:

input nodes for receiving input signals and an external signal;

a memory array for storing data;

a decoding circuit for decoding the input signals to access the data;

an output data path circuit connected to the memory array for transferring the data; and

a delay locked circuit connected to the input nodes and the data output path the delay locked circuit including:

a measuring unit located on a first path for generating a measured delay based on at least one measurement on timing of the external signal on the first path;

an interval controller located on the first path, the interval controller is configured to control a frequency of the measurement to be unequal to a frequency of the external signal; and

an adjusting unit located on a second path for delaying the external signal to generate and internal signal based on the measured delay, the adjusting unit including an output node connected to the output data path for providing the internal signal to the output data path circuit to control a transfer of the data between the memory array and the output data path circuit ~~The memory device of claim 5~~, wherein the interval controller includes a frequency modifier connected between the input nodes and the measuring [[uni]] unit for modifying the frequency of the external signal.

9. (Original) The memory device of claim 5, wherein the adjusting unit includes a plurality of correction delay elements connected between the input nodes of the memory device and the output nodes of the adjusting unit.

10. (Currently Amended) A memory device comprising:

input nodes for receiving input signals and an external signal;

a memory array for storing data;

a decoding circuit for decoding the input signals to access the data;

an output data path circuit connected to the memory array for transferring the data; and

a delay locked circuit for generating an internal signal based on the external signal, wherein the output data path circuit connects to the delay locked circuit for receiving the internal signal to control a transfer of data from the memory array, the delay [[lock]] <u>locked</u> circuit including:

a measuring unit located on a first path for generating a measured delay based on at least one measurement on timing of the external signal on the first path;

a frequency divider located on the first path for dividing a frequency of the external signal to control a frequency of the measurement such that the frequency of the measurement is unequal to the frequency of the external signal; and

an adjusting unit located on a second path for delaying the external signal to generate the internal signal based on the measured delay.

11. (Original) The memory device of claim 10, wherein the frequency divider includes:

a plurality of flip flops for producing a plurality of selectable signals with unequal frequencies; and

a selector connected to the flip flops for selecting one of the selectable signals to produce a measuring signal.

12. (Original) The memory device of claim 11, wherein the measuring unit includes a plurality of measuring delay elements for delaying the measuring signal.

13. (Original) The memory device of claim 12, wherein the measuring unit further includes a control logic connected to the plurality of measuring delay elements for stopping the measurement based on a shift signal produced from the measuring signal.

14. (Currently Amended) The memory device of claim 13, wherein the adjusting unit includes a plurality of correction delay elements for applying [[the]] a delay to the external signal.

15. (Currently Amended) A system comprising:

a processor;

a data bus connected to the processor for transferring data; and

a memory device connected to the data bus, the memory device including:

an input node for receiving an external signal;

a memory array having row and column of memory cells;

a row decoder connected to the memory device;

a column decoder connected to the memory device;

a plurality of measuring delay elements connected to the input node for delaying the external signal during a measurement to produce a measured delay, wherein the measurement is set to last for at least one cycle time of the external signal;

an interval controller connected between the input nodes and the measuring delay elements for controlling the frequency of the measurement;

a plurality of correction delay elements connected to the input node for delaying the external signal based on the measured delay to generate an internal signal; and

an output data path circuit connected to the memory array and the plurality of the correction delay elements for receiving the internal signal to control a timing of the data transferred on the data bus.

16. (Currently Amended) A system comprising:

a processor;

a data bus connected to the processor for transferring data; and

a memory device connected to the data bus, the memory device including:

an input node for receiving an external signal;

a memory array having row and column of memory cells;

a row decoder connected to the memory device;

a column decoder connected to the memory device;

a plurality of measuring delay elements connected to the input node for delaying the external signal during a measurement to produce a measured delay;

an interval controller connected between the input nodes and the measuring delay elements for controlling the frequency of the measurement;

a plurality of correction delay elements connected to the input node for delaying the external signal based on the measured delay to generate an internal signal; and

an output data path circuit connected to the memory array and the plurality of the correction delay elements for receiving the internal signal to control a timing of the data transferred on the data bus ~~The system of claim 15~~, wherein the interval controller includes a frequency modifier for setting a time interval between one measurement and the next measurement to be unequal to a cycle time of the external signal.

17. (Original) The system of claim 16, wherein the frequency modifier includes a frequency divider to divide the frequency of the external signal.

18. (Original) The system of claim 17, wherein interval controller further includes a frequency shifter for shifting signals produced by the frequency divider.

19. (Currently Amended) A method comprising:

receiving at a memory device input signals including an external signal;

propagating the external signal on a first signal path and on a second signal path;

performing a number of measurements on the first signal path to obtain a reference time based on a cycle time of the external signal, wherein a time interval between consecutive measurements among the number of measurements is unequal to the cycle time of the external

signal, and wherein at least one of the measurements lasts for at least one cycle time of the external signal;

generating a measured delay based on the reference time;

using the measured delay to adjust a delay applied to the external signal on the second signal path to generate an internal signal;

accessing data in a memory array of the memory device based on the input signals; and

transferring the data from the memory array to and output data path based on the internal signal.

20. (Original) The method of claim 19, wherein performing the number of measurements includes delaying the external signal for a portion of the cycle time of the external signal in each of the measurements.

21. (Original) The method of claim 19, wherein the measured delay represents a number of delay elements.

22. (Original) The method of claim 19, wherein the delay applied to the external signal on the second signal path equals the measured delay.

23. (Original) The method of claim 19, wherein the time interval between consecutive measurements among the number of measurements is greater than the cycle time of the external signal.

24. (Currently Amended) A method comprising:

providing an external signal to a memory device;

providing plurality of address signals to the memory device;

propagating the external signal through a number of measuring delay elements on a measuring path;

acquiring a measured delay by performing a first measurement on the measuring path, wherein the first measurement lasts for at least one cycle time of the external signal;

propagating the external signal through a number of correction delay elements on an output signal path to produce an internal signal;

adjusting a delay on the output signal path based on the measured delay;

performing a second measurement to adjust the signal relationship between the external and internal signals, wherein a time interval between the first measurement and the second measurement is unequal to the cycle time of the external signal;

accessing data in a memory array of the memory device based on the address signals; and

using the internal signal for outputting the data from the memory array to an output data path.

25. (Original) The method of claim 24, wherein performing the first measurement includes:

applying a model time delay to the measuring path;

producing a reference time based on a function of the model time delay and the cycle time of the external signal; and

converting the reference time to the measured delay.

26. (Currently Amended) A method comprising:

providing an external signal to a memory device;

providing plurality of address signals to the memory device;

propagating the external signal through a number of measuring delay elements on a measuring path;

acquiring a measured delay by performing a first measurement on the measuring path, wherein performing the first measurement includes applying a model time delay to the measuring path, producing a reference time based on a function of the model time delay and the cycle time of the external signal, and converting the reference time to the measured delay;

propagating the external signal through a number of correction delay elements on an output signal path to produce an internal signal;

adjusting a delay on the output signal path based on the measured delay;

performing a second measurement to adjust the signal relationship between the external and internal signals, wherein a time interval between the first measurement and the second measurement is unequal to the cycle time of the external signal;

accessing data in a memory array of the memory device based on the address signals; and

using the internal signal for outputting the data from the memory array to an output data path ~~The method of claim 25~~, wherein producing the reference time includes subtracting the model delay time from at least one cycle time of the external signal.

27. (Original) The method of claim 24, wherein adjusting the delay on the output path includes applying a correction delay equal to the measured delay to the output signal path.

28. (Currently Amended) A method comprising:

providing an external signal to a memory device;

providing plurality of row address signals to the memory device;

providing plurality of column address signals to the memory device;

propagating the external signal on a measuring path;

propagating the external signal on an output signal path to generate an internal signal;

periodically performing a measurement at a measuring frequency on the measuring path to synchronize the external and internal signals, wherein a frequency of the external signal is greater than the measuring frequency, wherein the measurement lasts for at least one cycle time of the external signal;

accessing data in a memory array of the memory device based on the row address signals and the column address signals; and

transferring the data from the memory array to and output data path based on the internal signal.

29. (Original) The method of claim 28, wherein periodically performing the measurement includes starting the measurement based on an edge of a start signal having a cycle time greater than the cycle time of the external signal.

30. (Currently Amended) A method comprising:

providing an external signal to a memory device;

providing plurality of row address signals to the memory device;

providing plurality of column address signals to the memory device;

propagating the external signal on a measuring path;

propagating the external signal on an output signal path to generate an internal signal;

periodically performing a measurement at a measuring frequency on the measuring path to synchronize the external and internal signals, wherein a frequency of the external signal is greater than the measuring frequency, wherein periodically performing the measurement includes starting the measurement based on an edge of a start signal having a cycle time greater than the cycle time of the external signal, and ~~The method of claim 29,~~ wherein periodically performing the measurement further includes stopping the measurement based on an edge of a stop signal, the stop signal being shifted from the start signal by at least one cycle of the external signal;

accessing data in a memory array of the memory device based on the row address signals and the column address signals; and

transferring the data from the memory array to and output data path based on the internal signal.

31. (Currently Amended) A method comprising:

providing an external signal to a memory device;

providing plurality of address signals to the memory device;

dividing a frequency of the external signal to produce a start signal;

propagating the start signal on a first signal path;

performing a first measurement on the ~~measuring~~ first signal path to acquire a measured delay, wherein the first measurement lasts for at least one cycle time of the external signal;

propagating the external signal on a second signal path to produce an internal signal;

applying the measured delay to the second path based on the measured delay;

performing a second measurement to adjust the signal relationship between the external and internal signals, wherein a time interval between the first measurement and the second measurement is unequal to the cycle time of the external signal;

accessing data in memory cells of the memory device based on the address signals; and

using the internal signal to control a transfer of the data between the memory cells and an output data path.

32. (Original) The method of claim 31, wherein the external signal has a frequency greater than a frequency of the start signal.

33. (Original) The method of claim 31, wherein the external signal has a frequency equal to a multiple of a frequency of the start signal.

34. (Original) The method of claim 31, wherein propagating the start signal on the first signal path includes propagating the start signal through a number of measuring delay elements.

35. (Original) The method of claim 34 wherein propagating the external signal on the second signal path includes propagating the external signal through a number of correction delay elements.

36. (Currently Amended) The method of claim 35, wherein [[a]] <u>the</u> number of measuring delay elements and [a]] <u>the</u> number of correction delay elements are equal.